WEST Search History

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DATE: Thursday, January 08, 2004

09 751750

Hide?	Set Name	Query	Hit Count
		DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=ADJ	
☐	L15	l13 and stop	0
☐	L14	l13 and type near stop	0
☐	L13	('4860290')!.PN.	2
☐	L12	('5737342' |'US20020087931A' |'20020087931' |'6184810')!.PN.	6
☐	L11	('5737342' |'US20020087931A' |'20020087931' |'6184810')!.PN.	6
☐	L10	on$1chip near test$3 with (clock or signature or switch$3 or select$3 or multiplex$3 or mux or filter$3 or weigh$4) with channel and pattern	4
☐	L9	on$1chip near test$3 with (clock or signature or switch$3 or select$3 or multiplex$3 or mux or filter$3 or weigh$4) with channel with pattern	0
☐	L8	('6243665')!.PN.	2
☐	L7	('6349392')!.PN.	2
☐	L6	l3 and scan$4 with stop$4 with test$3 same (bist or built$3 or self) and mask$3	5
☐	L5	l3 and scan$4 with stop$4 with test$3 same (bist or built$3 or self) andmask$3	0
☐	L4	l3 and scan$4 with stop$4 with test$3 same (bist or built$3 or self) same mask$3	0
☐	L3	l2 and scan$4 with stop$4 with test$3 same (bist or built$3 or self)	21
☐	L2	l1 and scan$4 with stop$4 with test$3	415
☐	L1	scan$4 with stop$4	20988

END OF SEARCH HISTORY

h e b b cg b chh e e f ff e ch e g e

First Hit Fwd Refs

Generate Collection

L6: Entry 4 of 5 File: USPT Jun 5, 2001

DOCUMENT-IDENTIFIER: US 6243665 B1
TITLE: Monitoring and control apparatus incorporating run-time fault detection by boundary scan logic testing

Detailed Description Text (27):
In addition, if enable/disable switch 16 is set in the disable position, the boundary scan test that uses boundary scan controller board 7 is stopped even if boundary scan controller board 7 is connected to system bus 2, and the normal test method of CPU board 4, such as a test according to a self-check, is performed to determine whether or not there is an abnormality in CPU board 4 itself and control board 5 and so forth.

Detailed Description Text (82):
In addition, in the case in which an integrated circuit has malfunctioned despite correct input data, the malfunction of the integrated circuit can be masked by transferring the contents of the cell provided on the input terminal side of this integrated circuit to the cell provided on the output terminal side.

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Hide?	Set Name	Query	Hit Count
		DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=ADJ	
☐	L11	l9 and raj$3 and level shift$3 and correlat$3	1
☐	L10	raj$3 and level shift$3 and correlat$3	1
☐	L9	raj$3 and level shift$3	46
☐	L8	raj$3 and level	8586
☐	L7	rajsky and level	0
☐	L6	rajky and level	0
☐	L5	rajky same level	0
☐	L4	('5737342' |'US20020087931A' |'20020087931' |'6184810')!.PN.	6
☐	L3	('5737342' |'US20020087931A' |'20020087931' |'6184810')!.PN.	6
☐	L2	on$1chip near test$3 with (clock or signature or switch$3 or select$3 or multiplex$3 or mux or filter$3 or weigh$4) with channel and pattern	4
☐	L1	on$1chip near test$3 with (clock or signature or switch$3 or select$3 or multiplex$3 or mux or filter$3 or weigh$4) with channel with pattern	0

END OF SEARCH HISTORY

h e b b cg b chh e e f ff e ch e g e